TELEDYNE e2v
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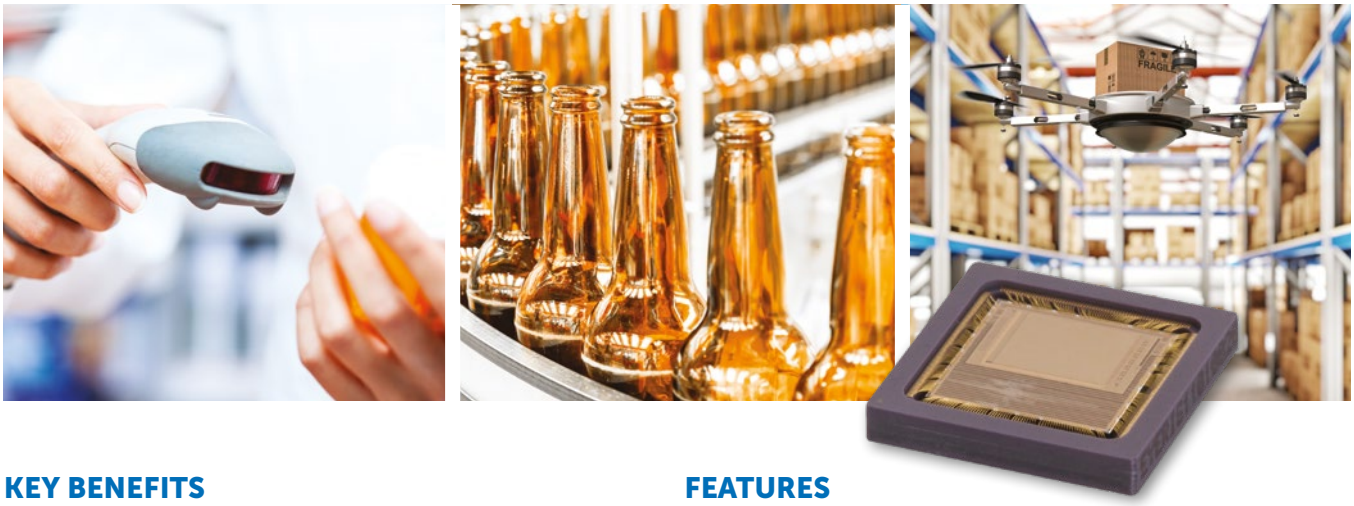
Part of the Teledyne Imaging Group

EYE-RIS VSOC
Patented smart image sensor technology, high speed Vision System on Chip

Paving the Way for Future Generations of Smart Sensors



KEY BENEFITS

- Single chip vision system embedding in-pixel processing circuitry allowing complex image sensing and processing at multi-thousand frames per second (fps)
- CMOS programmable Vision System on Chip (VSoC) optimized for industrial applications requiring image sensing, image processing, and decision making at extreme frame rates
- QCIF high speed image sensor processor
- Active pixels: 176 x 144
- On chip 32-bit RISC microprocessor for device control and image post processing
- On chip RAM for program and image/data storage
- Point to point, morphological, and statistical operations
- Spatial filtering, blob analysis and features extraction
- <2W power consumption @ 10,000fps (processing-dependent)

FEATURES

- Global shutter
- Multiple communication ports including UART, PWM (2 ports), USB2.0, JTAG, and several software configurable general purpose input/output ports for controlling external devices like illumination sources or engines
- 1cm^2 packaged size with 700mW power consumption at full speed operation

TYPICAL APPLICATIONS

- Automotive
- Machine vision
- Security
- Games
- Battery powered products

SENSOR OVERVIEW

The Eye-RIS smart sensor is a programmable, autonomous, and complete Vision-System-on-Chip (VSoC) using **Teledyne AnaFocus'** proprietary and patented Smart Image Sensor (SIS) technology. SIS technology extends the functionality of CMOS image sensors with the incorporation of image storage and advanced mixed-signal processing capabilities per pixel, enabling Eye-RIS to deliver image processing capabilities and speed comparable to a high end conventional vision system in a compact size with low power consumption and at a fraction of the cost.

The Eye-RIS VSoC includes a parallel CMOS image sensor processor with 32-bit RISC microprocessor performing post processing and system control tasks, several I/O and high speed communication ports that allow the system to communicate and/or to control external systems, and on chip memory. The combination of massive parallel image pre-processing in the sensor with complex image post-processing in the microprocessor results in ultra-compact implementation of a vision system able to perform complex machine vision algorithms at speeds of several thousands of images per second.

OPTICAL SPECIFICATIONS	
Image sensor	1cm² SIS CMOS
Sensing area – mm	4.8 (H) x 5.9 (V)
Cell size – µm	33.6 (SQ)
Pixel active area – µm	6 (SQ)
Active pixels	176 x 144
Responsivity – (DN8bits/µJ/cm²) @ 650nm (Max)	3.2
Dynamic range – dB	52
PRNU – %	1.2
DSNU – %	0.35
Digital video output	Monochrome, 8 bits
Programmable exposure	1µs to 20ms

IN-PIXEL PROCESSING
Storage of up to 7 gray level images and 4 binary images
Grayscale image arithmetic, image convolutions, and scale to binary conversion
Low pass, high pass, band pass, and stop band spatial filters with programmable bandwidth
HitAndMiss binary operations (3x3 binary pattern matching)
Active pixel detections
RoI-based processing

ON CHIP DIGITAL CONTROL AND MEMORY	
Altera Nios II 32-bit micro-processor	JTAG module
8+8k bytes of instruction and data cache	SPI interface for flash memory connection
256k bytes of SDRAM for program and data	Extension port for external SDRAM
128k bytes of SDRAM for image storage	

I/O AND INTERFACES	
On chip bank of 4 ADCs and 4 DACs (8-bit at 50MHz) for grayscale image I/Os	Specific compressed I/O modes: image mean, number of pixels, coordinates of pixels
16-bit GPIO	x2 PWM ports
UART	FIFO interface for image and data I/O

MISCELLANEOUS	
Power supply– V	Dual 3.3 and 1.8
Power – W	<2 @ 10,000fps (processing dependent) acquiring and reading out images to external memory. USB interface and 4GPIOs are considered to be active
Operating humidity – %	20 – 80 non-condensing
Storage temperature/ humidity	-10°C to 60°C/20 – 80%
Package	218 pin LGA, ceramic